ELECTRONIC MATERIALS

Two-dimensional indium selenide wafers for integrated electronics

Biao Qin[1,2]†, Jianfeng Jiang[3]*†, Lu Wang[4], Quanlin Guo[1,5], Chenxi Zhang[3], Lin Xu[3], Xing Ni[4], Peng Yin[2], Lian-Mao Peng[3], Enge Wang[6,7], Feng Ding[8], Chenguang Qiu[3]*, Can Liu[2]*, Kaihui Liu[1,6,9]*

Two-dimensional (2D) indium selenide, with its low effective mass, high thermal velocity, and exceptional electronic mobility, is a promising semiconductor for surpassing silicon electronics, but grown films have not achieved performance comparable with that of exfoliated micrometer-scale flakes. We report a solid–liquid–solid strategy that converts amorphous indium selenide films into pure-phase, high-crystallinity indium selenide wafers by creating an indium-rich liquid interface and maintaining a strict 1:1 stoichiometric ratio of indium to selenium. The as-obtained indium selenide films exhibit exceptional uniformity, a pure phase, and a high crystallinity across an entire ~5-centimeter wafer. Transistor arrays based on the produced indium selenide wafers demonstrate outstanding electronic performance surpassing that of all 2D film-based devices, including an extremely high mobility (averaging as high as 287 square centimeters per volt-second) and a near-Boltzmann-limit subthreshold swing (averaging as low as 67 millivolts per decade) at room temperature.

Advancements in artificial intelligence and Internet of Things technologies have imposed substantial demands on computational power (*1*). However, silicon-based transistor technology is approaching its intrinsic physical limits at sub–10-nm nodes, restricting further improvements in the chip performance, power efficiency, and integration density (*2*, *3*). New semiconductor channel materials that can overcome the limitations of silicon, thereby sustaining further growth in the transistor density for future integrated circuit nodes, are needed (*4*–*7*).

Two-dimensional (2D) atomically thin semiconductors—such as molybdenum disulfide (MoS_2), tungsten disulfide (WS_2), tungsten diselenide (WSe_2), black phosphorus, bismuth oxyselenide (Bi_2O_2Se), and indium selenide (InSe)—are candidates for sub–3-nm technology nodes (*8*–*17*). Among them, InSe is a 2D semiconductor that theoretically could surpass silicon limits because of its low effective mass [$0.14m_0$, compared with $0.19m_0$ for silicon and 0.3 to $0.6m_0$ for transition-metal dichalcogenides (TMDs), where m_0 is the electron mass], high thermal velocity (>1.3 cm/s, compared with 1.2 cm/s for silicon and <0.8 cm/s for TMDs), theoretically high mobility (1000 $cm^2/V{\cdot}s$ at room temperature), and appropriate bandgap (>1.26 eV, compared with 1.12 eV for silicon) (*17*, *18*). This exceptional performance has recently been demonstrated for exfoliated microscale InSe flakes (*19*), but the scalability of integrated electronics based on a vast number of devices ultimately relies on large-scale, high-quality InSe wafers.

Currently, wafer-scale InSe films are primarily produced through various thin-film deposition techniques, such as metal-organic chemical vapor deposition and molecular beam epitaxy, but the performance of the grown films is decreased so that they underperform compared with 2D TMD semiconductors (*20*–*23*). The main challenge in high-quality InSe film growth arises for two main reasons. First, the phase diversity within the In-Se system is complex because there are at least four stable phases (InSe, In_2Se_3, In_4Se_3, and In_6Se_7). Even slight compositional variations can trigger unwanted phase transitions that lead to considerable performance deviation and degradation (*22*). Second, the crystallinity of InSe films is poor because of the difficulty in maintaining a stoichiometric balance between In and Se because the vapor pressure of Se is approximately seven orders of magnitude greater than that of In at a growth temperature of ~500°C (*24*). Achieving a pure-phase, high-crystallinity film is a critical prerequisite for unlocking the full potential of InSe wafers in large-scale integrated electronics.

Design and growth

To prevent the formation of other phases, we maintained a strict 1:1 stoichiometric ratio of In to Se by sealing a predeposited amorphous InSe wafer. A high-purity InSe target was used in magnetron sputtering to uniformly deposit the amorphous InSe film onto a ~5-cm sapphire substrate (Fig. 1A and fig. S1). This amorphous InSe wafer was placed into a custom steel groove, covered with fused silica, and sealed at the edges with liquid In (with a melting point of ~157°C). This configuration created a sealed space that prevented atomic loss during growth at a high temperature of ~550°C and maintained the stoichiometric ratio of In to Se in the InSe film [Fig. 1B and supplementary materials (SM) materials and methods].

High crystallinity was achieved with a solid–liquid–solid (SLS) growth mechanism, in which recrystallization of amorphous InSe occurred at an In-rich liquid interface. Trace amounts of additional In atoms were introduced by the surrounding liquid In and the saturated In vapor in the reactor to facilitate the formation of a liquid In-rich interface (Fig. 1C and fig. S2) (*25*). Our density functional theory calculations showed that the formation energy of amorphous InSe was ~0.38 eV/atom greater than that of the crystalline InSe, so the transformation from amorphous to crystalline InSe would be energetically preferred (fig. S3). With a liquid In-rich interface, the In and Se atoms of the amorphous InSe quickly dissolved into the liquid interface and then precipitated out on the crystalline InSe side, which kinetically promoted the structural transformation (Fig. 1D and fig. S4). To verify the SLS mechanism, we carefully examined the interface between amorphous and crystalline InSe. The In-rich interface was clearly visualized in the cross-sectional scanning transmission electron microscopy (STEM) images and further confirmed with corresponding fast Fourier transform (FFT) patterns (Fig. 1E).

High crystallinity of InSe wafers

We experimentally prepared ~5-cm high-quality InSe wafers on sapphire substrates through the proposed strategy (Fig. 2A). The thickness of the InSe films was nearly linearly dependent on the sputtering time, with a slope of ~0.28 layers per second (fig. S5). In our current experimental configuration, the minimum achievable thickness was ~2.5 nm (three layers), which was mainly constrained by the limitations of the magnetron sputtering technique (fig. S6). When the film thickness reaches ≥30 nm, the vertical penetration of liquid In becomes insufficient to achieve full crystallization of the InSe layers (fig. S7). The crystallization of the InSe film was evident from the reduction in the surface roughness from ~415 pm in the amorphous state to only ~37 pm in the crystalline state (Fig. 2B and fig. S8). In addition, the uniform contrast in the optical

[1]State Key Laboratory for Mesoscopic Physics, Frontiers Science Centre for Nano-optoelectronics, School of Physics, Peking University, Beijing, China. [2]Key Laboratory of Quantum State Construction and Manipulation (Ministry of Education), School of Physics, Renmin University of China, Beijing, China. [3]Key Laboratory for the Physics and Chemistry of Nanodevices and Center for Carbon-based Electronics, School of Electronics, Peking University, Beijing, China. [4]Institute of Functional Nano & Soft Materials (FUNSOM) and Jiangsu Key Laboratory of Advanced Negative Carbon Technologies, Soochow University, Suzhou, China. [5]Interdisciplinary Institute of Light-Element Quantum Materials and Research Centre for Light-Element Advanced Materials, Peking University, Beijing, China. [6]International Centre for Quantum Materials, Collaborative Innovation Centre of Quantum Matter, Peking University, Beijing, China. [7]Tsientang Institute for Advanced Study, Hangzhou, China. [8]Suzhou Laboratory, Suzhou, China. [9]Songshan Lake Materials Laboratory, Dongguan, China. ***Corresponding author. Email: canliu@ruc.edu.cn (C.L.); jjf19950926@gmail.com (J.J.); chenguangqiu@pku.edu.cn (C.Q.); khliu@pku.edu.cn (K.L.)** †These authors contributed equally to this work.

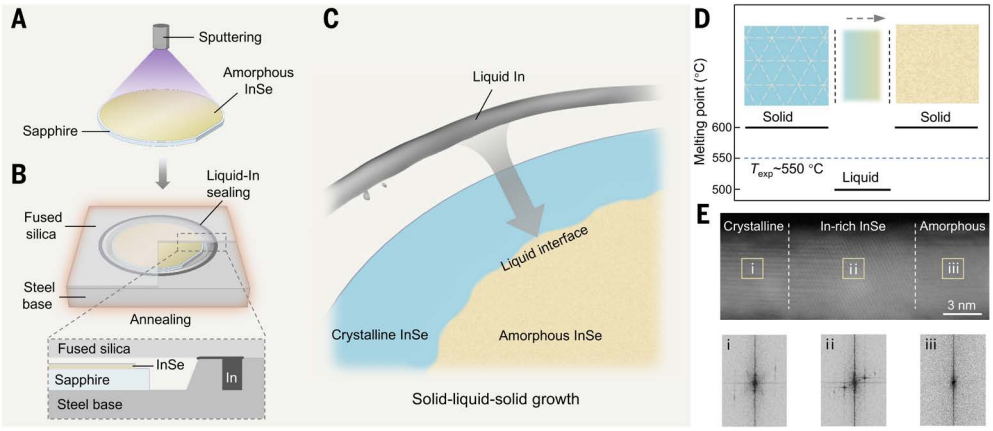

Fig. 1. Design of the SLS strategy for InSe wafer growth. (**A**) Amorphous InSe films are deposited on a single-crystal sapphire substrate by means of magnetron sputtering. (**B**) Schematic of the annealing device designed to hold a ~5-cm wafer. In the main structure, the central groove in the steel base holds the wafer, whereas the surrounding groove (1 mm deep) contains liquid In. A fused silica plate was placed on top of the steel base. Liquid In was used to seal InSe wafers. (**C**) Zoomed-in diagram of the SLS growth in (B). Liquid In evaporated to create an In-rich interface between amorphous and crystalline InSe. At this interface, the amorphous solid continuously transformed into a crystalline InSe film. (**D**) Schematic of SLS evolution. At the experimental temperature (T_{exp} ~ 550°C), only the In-rich interface is in liquid state, promoting recrystallization by enhancing atomic diffusion and lowering the formation energy. (**E**) Cross-sectional STEM image and corresponding FFT patterns, showing the presence of the In-rich interface between amorphous and crystalline InSe regions.

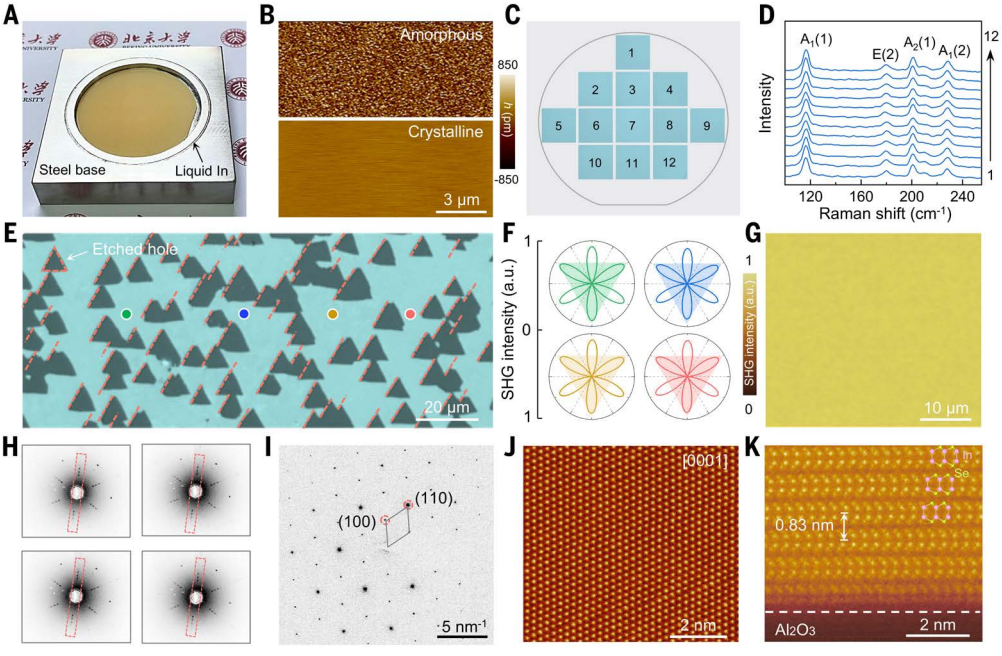

Fig. 2. Characterizations of InSe films. (**A**) Photograph of an as-grown 10-nm-thick InSe film on a ~5-cm sapphire substrate positioned in the steel base. (**B**) Atomic force microscopy roughness (standard deviation of the height, *h*) images of (top) amorphous and (bottom) crystalline InSe. (**C**) Optical images of an as-grown InSe film collected from 12 representative areas on a ~5-cm wafer. All the images are of the same size (150 by 150 μm). (**D**) Raman spectra of InSe collected at the corresponding areas in (C), indicating the uniformity of the as-grown InSe film. (**E**) Optical images of InSe films after H_2 etching. The etched holes all had triangular shapes and the same orientation. (**F**) Polarization-dependent SHG patterns of InSe in the corresponding areas marked in (E). (**G**) SHG mapping of the InSe film. (**H**) LXD patterns of an InSe film at four different positions. The size of the x-ray spot was ~0.2 mm. (**I**) SAED patterns of the InSe film. (**J**) HAADF-STEM image of the InSe film. (**K**) Cross-sectional HAADF-STEM image of as-grown InSe on sapphire substrate, revealing the ABC stacking order.

images and nearly identical Raman spectra collected from 12 representative areas evenly distributed across the ~5-cm InSe wafer consistently demonstrated its large-area uniformity (Fig. 2, C and D). Our methodology is fundamentally scalable for the production of large InSe wafers, as demonstrated by the highly uniform ~10-cm wafer (fig. S9).

To evaluate the crystallinity of the grown InSe film, we used H_2 etching to visualize its crystallographic orientation. Because of the threefold symmetry (C_{3v}) of InSe, triangular holes with a uniform orientation consistently appeared, providing strong evidence of the single-crystal structure of the film across a large area (Fig. 2E and fig. S10). Additionally, the highly consistent polarization-dependent second-harmonic generation (SHG) patterns, along with the uniform intensity distribution in the SHG mapping, further validated the monocrystalline nature of the InSe film (Fig. 2, F and G). Furthermore, Laue x-ray diffraction (LXD) patterns (x-ray spot of ~0.2 mm) measured at four different positions across a 1- by 1-cm region revealed sharp and consistently arranged spots, confirming the high crystallinity on a large scale (Fig. 2H).

The detailed atomic structures of the InSe films were characterized by using selected-area electron diffraction (SAED) and high-angle annular dark-field STEM (HAADF-STEM). The SAED pattern with an incident zone axis of ⟨001⟩ clearly showed the intensities of representative diffraction spots (Fig. 2I), revealing the high crystallinity of the InSe lattice. Specifically, the lattice spacings of InSe are 0.34 and 0.21 nm, corresponding to the (100) and (110) planes, respectively, as reported in a previous study of single-crystal flakes (*26*). The triangular lattice of InSe was clearly visualized through the in-plane HAADF-STEM image, in which each atomic column represents a series of stacked In_2 + Se_2 (Fig. 2J and fig. S11). The out-of-plane view revealed a well-defined atomic structure with a layer spacing of 0.83 nm, in which each InSe layer is aligned in the same direction and followed a rhombohedral (ABC) stacking order (Fig. 2K and fig. S12). These results demonstrate that the InSe film had high crystallinity and quality.

Electronic performance of wafer-scale InSe transistor arrays

To further evaluate the crystalline quality of the InSe films, we fabricated large-scale integrated arrays of field-effect transistors (FETs) directly on sapphire substrates using the as-obtained 5-nm-thick InSe wafers for reliable statistical analysis of the electrical performance. A schematic of the devices is shown in Fig. 3A. To avoid the Fermi-level pinning effect, we used rare-earth yttrium (Y) doping in the contact metallization layer to achieve robust ohmic contact in wafer-scale InSe device arrays (*19*). Additionally, ultrathin 2.6-nm hafnium oxide (HfO_2) was

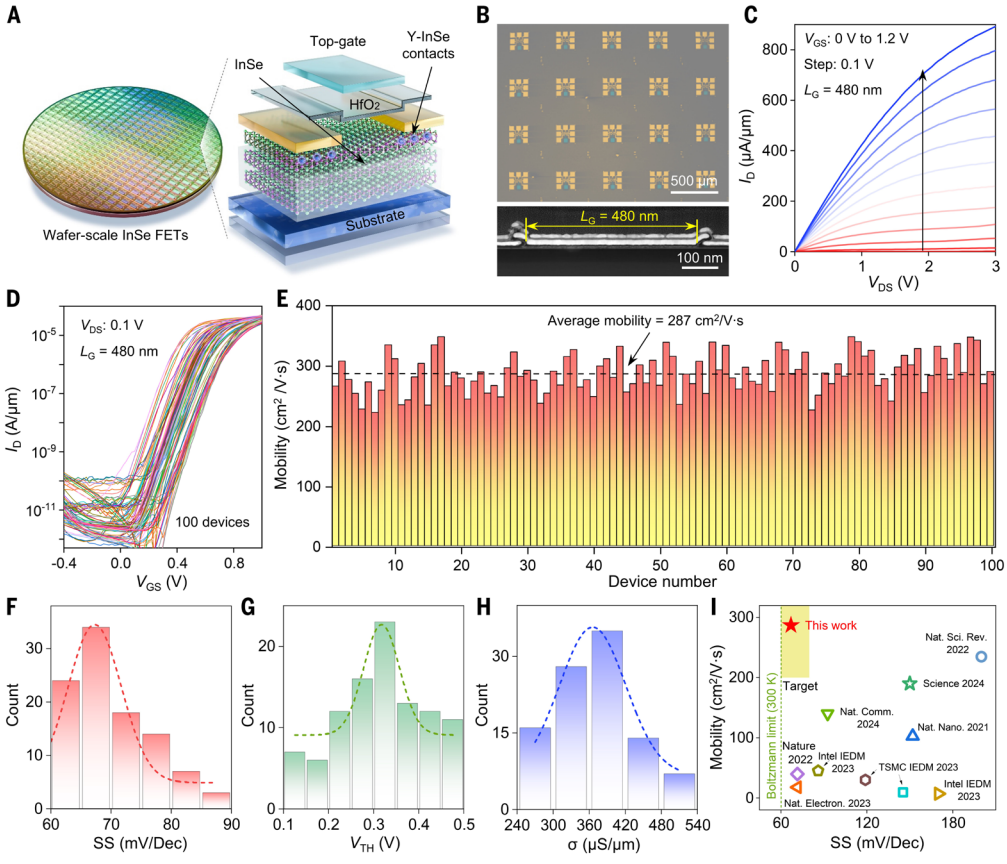

Fig. 3. Wafer-scale fabrication and statistics of the electrical performance of 2D InSe FETs. (**A**) Schematic diagram of wafer-scale InSe FETs with Y-doping–induced contact metallization. The purple, green, and blue spheres indicate In, Se, and Y atoms, respectively. (**B**) (Top) False-color SEM image and (bottom) typical cross-sectional STEM image of the top-gate InSe FET arrays on sapphire. (**C**) Typical output characteristic curve of the InSe FET with gate length L_G of 480 nm. (**D**) Transfer characteristics of 100 individual fabricated 2D InSe FET devices. (**E**) Statistical histogram of the field-effect mobility values from 100 individual 2D InSe FET devices. (**F** to **H**) Statistical distributions of the (F) SS, (G) threshold voltage V_{TH}, and (H) electric conductance σ of 100 individual 2D InSe FETs, revealing mean values of 67.3 mV per decade, 0.31 V, and 369 μS/μm, respectively. The dashed lines are Gaussian fitting curves. (**I**) Comparison of the mobility versus SS plots of our wafer-scale 2D InSe FETs (red star) with those of other reported film-based 2D counterparts (open symbols) (SM materials and methods, section S1.5, and references therein).

used as the top dielectric layer (SM materials and methods). In Fig. 3B, we show a false-colored scanning electron microscopy (SEM) image of the 2D InSe FET integrated array and a cross-sectional STEM image of a typical top-gate device with a gate length of 480 nm. Under a source-drain voltage (V_{DS}) of 3 V, with a gate-source voltage (V_{GS}) of 1.2 V, the corresponding saturation current density reached 892 μA/μm, which far exceeds that of any reported similarly sized 2D semiconductor devices for grown films (Fig. 3C).

The transfer characteristics of 100 individual InSe transistors at V_{DS} of 0.1 V are shown in Fig. 3D, and the field-effect mobility distribution is illustrated in Fig. 3E. The average field-effect mobility was 287 cm^2/V·s, with a peak mobility as high as 347 cm^2/V·s, which is higher than those of all other reported film-based 2D devices (figs. S13 and S14) (*27*, *28*). Additionally, these values meet the International Roadmap for Devices and Systems (IRDS) requirements for channel mobility in very-large-scale integration (*2*). Statistical histograms of the subthreshold swing, threshold voltage (V_{TH}), and electrical conductance (σ) are presented in Fig. 3, F to H, showing that the mean values of SS, V_{TH}, and σ are 67.3 mV per decade, 0.31 V, and 369 μS/μm, respectively. In Fig. 3I, the benchmark plot of the mobility versus the SS demonstrates the advantage of our InSe devices in both the switching speed and mobility compared with those of other reported devices.

Ballistic transport performance of 10-nm InSe transistors

The ballistic transport performance in ultrashort-channel 2D devices offers another robust assessment measure beyond the mobility to evaluate the wafer quality in advanced technology nodes below 10 nm. We fabricated ballistic InSe transistors with a channel length of 10 nm (Fig. 4A) using Y-doping contacts and a dual-gate structure to enhance gate efficiency by transferring the films from sapphire to Si substrates (fig. S15 and SM materials and methods). The cross-sectional structure and elemental distribution of the devices were determined by using STEM and electron energy-loss spectroscopy (EELS) (Fig. 4B). The back-gate length was 10 nm, whereas the top-gate length was 5 nm, with the channel comprising three layers of InSe. Both the top- and back-gate dielectrics were composed of ~2.6-nm-thick HfO_2.

The transfer characteristics of a representative ballistic InSe transistor are shown in Fig. 4C, demonstrating nearly ideal switching behavior, with an SS as low as 79 mV per decade and a switching current ratio exceeding 10^7, which meets the stringent requirements for advanced logic circuits. Additionally, the device operates at an ultralow voltage of 0.5 V, with its off-state current satisfying the IRDS requirements for high-performance and high-density applications. The on/off ratio versus the drain current (I_D) illustrates that the comprehensive switching characteristics of our device surpassed those of other 2D counterparts by at least two orders of magnitude (Fig. 4D) (*29*–*31*).

The output characteristics of a representative 10-nm InSe transistor are presented in Fig. 4E, which displays a saturation current density of up to 1.2 mA/μm at 0.8-V V_{DS} and 1.0-V V_{GS}, and a standard current density of 1 mA/μm was achieved at an ultralow V_{DS} of 0.46 V. Because of the high-quality InSe channel material, Y-doped metallic ohmic contacts, and efficient dual-gate architecture, our ballistic InSe device exhibited superior comprehensive electrical characteristics across six key parameters—operating voltage, gate length, drain-induced barrier lowering (DIBL), effective mass, on/off ratio, and ballistic ratio—compared with Intel 3 technology nodes and state-of-the-art film-based 2D transistors (Fig. 4F) (*32*–*35*). Its overlap-free intrinsic gate delay was as low as 0.39 ps, and its energy-delay product (EDP) reached a particularly low value of 5.27×10^{-29} J·s/μm, exceeding the predicted limits for silicon-based technologies outlined in the IRDS until 2037 (Fig. 4G) (*2*).

Discussion and outlook

We have developed a SLS strategy to produce high-quality InSe films at the wafer scale. These films exhibit exceptional uniformity and crystallinity, which enables outstanding transistor array performance, including a record high mobility and a near-Boltzmann-limit

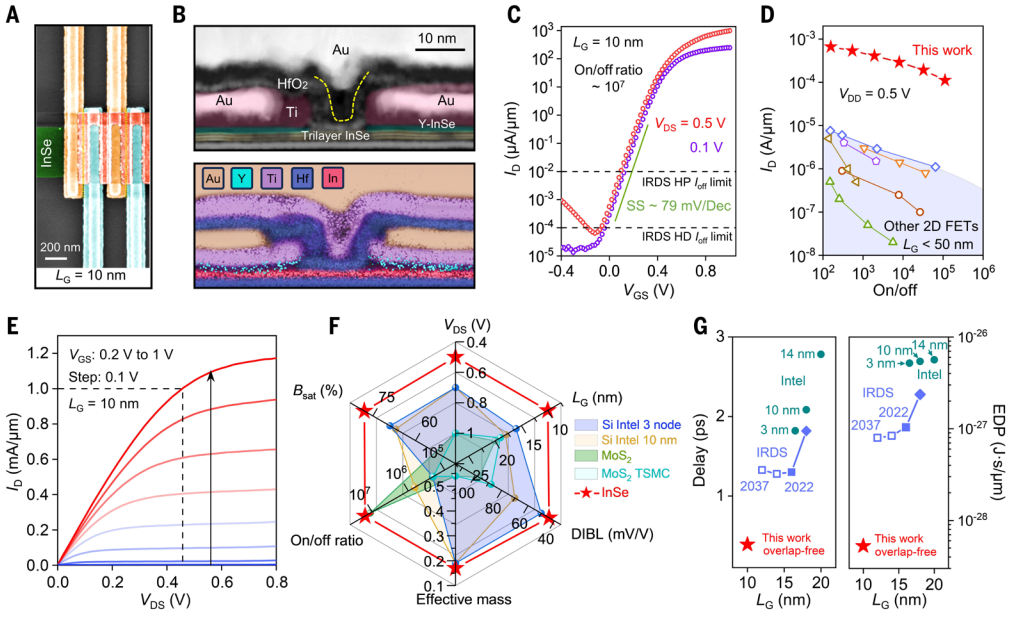

Fig. 4. Short-channel electrical performance and benchmarking of InSe FETs. (**A**) Top-view SEM image of a typical fabricated ballistic 2D trilayer InSe FET with a 10-nm gate length. (**B**) (Top) Cross-sectional STEM image of a ballistic trilayer InSe FET featuring a highly efficient dual-gate structure. (Bottom) The EELS maps illustrate the spatial distributions of gold (Au), Y, titanium (Ti), hafnium (Hf), and In, confirming the locations of the 2D InSe channel, electrode, and gate stack. (**C**) Transfer characteristics of a typical ballistic double-gate InSe FET with a 10-nm gate length. (**D**) Comparison of the on-state current (I_D) versus the on/off ratio of our typical ballistic trilayer double-gate InSe FETs (red stars) with that of other short-channel ($L_G < 50$ nm) 2D counterparts (light blue shaded area). The I_D and corresponding on/off ratio are defined within a 0.5-V window along each transfer curve. (**E**) Output characteristic curves of the ballistic 2D InSe FET with L_G of 10 nm. (**F**) Radar plot of the electrical performance of our InSe FETs versus other reported short-channel FETs, including key parameters such as V_{DS} (reaching a standard saturation current density of >1 mA/μm), L_G, DIBL, effective mass, on/off ratio, and ballistic ratio (B_{sat}). TSMC, Taiwan Semiconductor Manufacturing Company. (**G**) Scaling trends of (left) intrinsic gate delay and (right) EDP of our ballistic 2D InSe FETs with an overlap-free architecture compared with those of silicon.

SS for large-scale 2D devices. Ultrashort-channel (10-nm) InSe transistors demonstrate key parameters—including the operating voltage, gate length, DIBL, effective mass, on/off ratio, and ballistic ratio—that exceed those of the current state-of-the-art Intel 3-nm-node technology. The delay and EDP of the device fall below the 2037 IRDS predicted limits for silicon technology. We anticipate that integrated electronics produced from 2D InSe wafers will drive the development of advanced transistors, offering a more flexible, low-power, high-performance solution for next-generation computing and communication technologies.

REFERENCES AND NOTES

1. T. N. Theis, H. S. P. Wong, *Comput. Sci. Eng.* **19**, 41–50 (2017).
2. IEEE International Roadmap for Devices and Systems 2023 Update; https://irds.ieee.org/editions/2023.
3. W. Cao *et al.*, *Nature* **620**, 501–515 (2023).
4. D. Akinwande *et al.*, *Nature* **573**, 507–518 (2019).
5. Y. Liu *et al.*, *Nature* **591**, 43–53 (2021).
6. M. Chhowalla *et al.*, *Nat. Chem.* **5**, 263–275 (2013).
7. A. D. Franklin, M. C. Hersam, H. P. Wong, *Science* **378**, 726–732 (2022).
8. L. Li *et al.*, *Nat. Nanotechnol.* **9**, 372–377 (2014).
9. M. Y. Li, S. K. Su, H. P. Wong, L. J. Li, *Nature* **567**, 169–170 (2019).
10. T. Li *et al.*, *Nat. Nanotechnol.* **16**, 1201–1207 (2021).
11. K. C. Zhu *et al.*, *Nat. Electron.* **4**, 775–785 (2021).
12. J. Wang *et al.*, *Nat. Nanotechnol.* **17**, 33–38 (2022).
13. R. Wu *et al.*, *Nat. Electron.* **5**, 497–504 (2022).
14. J. H. Fu *et al.*, *Nat. Nanotechnol.* **18**, 1289–1294 (2023).
15. K. P. O'Brien *et al.*, *Nat. Commun.* **14**, 6400 (2023).
16. C. Tan *et al.*, *Nature* **616**, 66–72 (2023).
17. D. A. Bandurin *et al.*, *Nat. Nanotechnol.* **12**, 223–227 (2017).
18. E. G. Marin, D. Marian, G. Iannaccone, G. Fiori, *IEEE Electron Device Lett.* **39**, 626–629 (2018).
19. J. Jiang, L. Xu, C. Qiu, L. M. Peng, *Nature* **616**, 470–475 (2023).
20. Z. Yang *et al.*, *ACS Nano* **11**, 4225–4236 (2017).
21. J. Kang *et al.*, *Adv. Mater.* **30**, e1802990 (2018).
22. S. Song *et al.*, *Matter* **6**, 3483–3498 (2023).
23. H.-C. Chang *et al.*, *Small* **14**, e1802351 (2018).
24. C. H. Wu *et al.*, *Nanomaterials* **12**, 2435 (2022).
25. H. Bergeron *et al.*, *Appl. Phys. Rev.* **7**, 041402 (2020).
26. J. F. Jiang *et al.*, *Small Methods* **4**, 2000238 (2020).
27. G. Xue *et al.*, *Chem. Rev.* **124**, 9785–9865 (2024).
28. L. Liu *et al.*, *Nature* **605**, 69–75 (2022).
29. C. S. Pang, P. Wu, J. Appenzeller, Z. Chen, in *2020 IEEE International Electron Devices Meeting (IEDM)* (IEEE, 2020), pp. 3.4.1–3.4.4.
30. A. Nourbakhsh *et al.*, *Nano Lett.* **16**, 7798–7806 (2016).
31. S. B. Desai *et al.*, *Science* **354**, 99–102 (2016).
32. W. Li *et al.*, *Nature* **613**, 274–279 (2023).
33. W. C. Wu *et al.*, in *2024 IEEE Symposium on VLSI Technology and Circuits* (IEEE, 2024), pp. 1–2.
34. W. Hafez *et al.*, in *2024 IEEE Symposium on VLSI Technology and Circuits* (IEEE, 2024), pp. 1–2.
35. C. Auth *et al.*, in *2017 IEEE International Electron Devices Meeting (IEDM)* (IEEE, 2017), pp. 29.1.1–29.1.4.

ACKNOWLEDGMENTS

Funding: This work was supported by the National Natural Science Foundation of China (52025023, 52322205, 12274456, 52250398, T2188101, 51991342, 92163206, 11888101 62122006, and 92477201), National Key R&D Program of China (2022YFA1403500, 2022YFA1405600, 2021YFA1400502, and 2021YFA0717400), Guangdong Major Project of Basic and Applied Basic Research (2021B0301030002), Beijing Municipal Science and Technology Project (Z221100005822003), and Strategic Priority Research Program of Chinese Academy of Sciences (XDB3300000). This work has been supported by the New Cornerstone Science Foundation through the XPLORER PRIZE and Hangzhou Tsientang Education Foundation. **Author contributions:** K.L., C.L., and C.Q. supervised the project. K.L., C.L., C.Q., J.J., and B.Q. conceived the experiments. B.Q., X.N., L.W., C.L., F.D., and K.L. developed the growth mechanism. B.Q. conducted the growth experiments. J.J., C.Z., L.X., and C.Q. fabricated InSe devices and performed the electrical measurements and VS model simulation. B.Q., Q.G., C.Z., and P.Y. performed the SHG, Raman, PL, LXD, STEM, SEM, magnetron sputtering, and XRD experiments. B.Q., J.J., C.L., C.Q., and K.L. wrote the article. C.Q., K.L., L. P., and E.W. revised the manuscript. All the authors discussed the results and revised the paper. **Competing interests:** A Chinese patent application (no. 202510419972.2) related to this article was submitted by Peking University (K.L., C.L., and B.Q.). All other authors declare that they have no competing interests. **Data and materials availability:** All data are available in the main text or the supplementary materials.

SUPPLEMENTARY MATERIALS

science.org/doi/10.1126/science.adu3803
Materials and Methods; Figs. S1 to S15; References (*36*–*53*)

Submitted 8 November 2024; accepted 14 May 2025

10.1126/science.adu3803